

May 1999, ver. 6

Overview

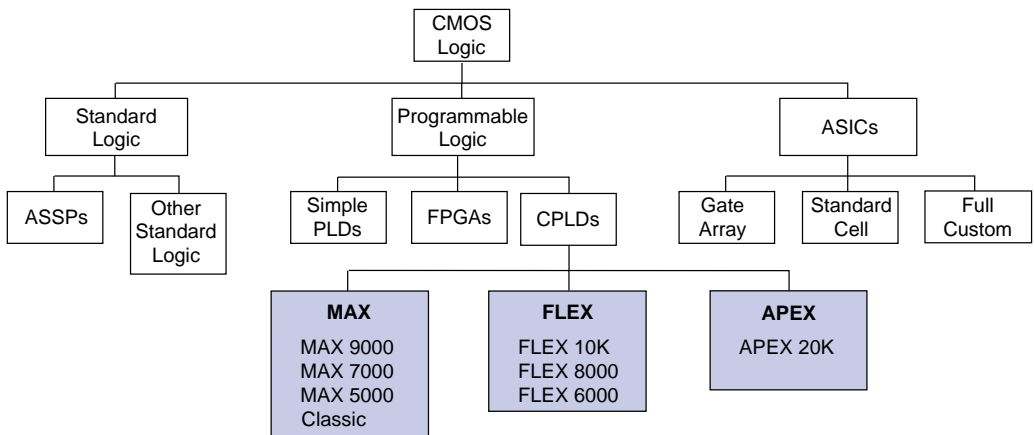
Designers today are challenged with producing quality products in a faster time frame and at lower costs than ever before. Altera offers a complete solution to help designers meet their customers' demands. Altera's System-on-a-Programmable-Chip™ solution combines programmable logic devices (PLDs), advanced development tools, and intellectual property (IP) to create a complete solution for all design needs. With multi-million gate PLDs, design issues become very complex. Altera PLDs provide the speed and density to address even the most difficult design problems. To support faster design cycles and streamline development, Altera offers state-of-the-art development software. As the multi-million gate programmable logic device (PLD) era approaches, the importance of solid technical and intellectual support becomes more evident. To further increase efficiency, Altera offers a full range of megafunctions to eliminate common programming tasks, allowing designers to focus on task-specific device functions. These features combine to give designers complete control over the development process.

Programmable Logic & ASICs

Programmable logic devices are standard, off-the-shelf user-configurable integrated circuits (ICs) used to implement custom logic functions. In the early 1980s, simple PLDs were typically used to integrate multiple discrete logic devices and designs were typically expressed using Boolean equations. Today, high-density PLDs are employed for system-level integration and are often a preferred alternative to application-specific integrated circuits (ASICs) or application-specific standard products (ASSPs). An ASIC is "custom designed" for each individual application; an ASSP is an off-the-shelf device that implements a specific function. Due to PLD cost decreases through high-volume manufacturing and the use of aggressive process technologies, Altera offers devices that are similar in integration, density, performance, and cost to that of an ASIC solution. These factors, combined with the time-to-market and flexibility of a programmable solution, continue to drive the increasing use of high density PLDs in the development and production of electronic systems.

Programmable logic encompasses all digital logic circuits configured by the end user, including simple, low-density, 20-pin PAL/GAL devices, field-programmable gate arrays (FPGAs), and complex PLDs (CPLDs). PLDs are offered in different architectures, and a variety of memory elements are available for device configuration. Altera PLDs are the fastest and largest in the industry. They offer densities and speeds approaching those of mainstream ASICs while avoiding the high up-front costs, large production commitments, and risks that are typically associated with the ASIC market. These PLDs also provide a high degree of flexibility, particularly when it comes to last-minute design changes. The combination of speed, flexibility, and reduced risk makes programmable logic an ideal design solution for today's electronic applications. Figure 1 shows the relationship of Altera products to CMOS logic products.

Figure 1. CMOS Logic Products



CPLDs and FPGAs have different interconnect structures. The segmented interconnect structure of FPGAs uses multiple metal lines of varying lengths, joined by pass transistors or anti-fuses, to connect logic cells. In contrast, the continuous interconnect structure of CPLDs uses continuous metal lines to provide logic cell-to-logic cell connectivity, which ultimately leads to higher speeds and smaller die sizes than comparable FPGAs. Additionally, the continuous interconnect structure eliminates the unpredictable timing associated with a segmented interconnect structure, and provides fast, fixed delay paths between logic cells by providing predictable timing. The continuous interconnect structure makes it easier to implement a design, and thus shortens the development cycle.

Advantages of Altera PLDs

Designers generally develop a logic circuit with one of three distinctly different implementation options: standard logic (ASSPs or other standard logic devices), custom or semi-custom devices (ASICs), or PLDs. The best option is one that can meet the largest number of design requirements. Table 1 lists a number of important requirements and rates the three options according to their effectiveness in meeting these requirements.

Requirement	PLD	ASIC
Speed	●	●
Density	●	●
Cost	●	● (2)
Development time	●	○
Prototyping and simulation time	●	○
Manufacturing time	●	○
Ease of use	●	○
Future modification	●	○
Inventory risk	●	○
Development tool support	●	●

Notes:

- (1) ● Very effective
○ Poor
- (2) Cost-effective only in very high-volume production quantities.

Altera devices offer the general benefits of PLDs as well as innovative architectures, advanced process technologies, state-of-the-art development tools, and a wide selection of megafunctions. The advantages of Altera PLDs include:

- High performance
- High-density logic integration
- Cost-effectiveness
- Short development cycles with the Quartus™ and MAX+PLUS® II development software
- Megafunctions optimized for Altera devices
- Benefits of in-system programmability (ISP) and in-circuit reconfiguration (ICR)

High Performance

Performance is a function of technology and architecture. Because Altera devices are manufactured on state-of-the-art CMOS processes, they offer the fastest possible performance. In addition, continuous interconnect structures provide fast, consistent signal delays throughout the device, and innovations such as specialized on-chip circuitry further enhance system performance.

High-Density Logic Integration

Designers often seek the highest possible logic integration for new designs, usually to reduce board space and cost. Also, existing designs frequently undergo secondary development cycles in the attempt to reduce cost by integrating more logic into fewer devices. In both cases, PLDs with a high logic integration capability offer an excellent solution. Altera devices—which range in density from 300 to 1 million typical gates—can easily integrate existing logic, including small and large numbers of standard logic devices, PLDs, FPGAs, or custom devices. The high integration capability of PLDs provides higher system performance, greater reliability, and lower system cost. Altera APEX® devices have high densities, which makes them ideal for applications that have been historically implemented with ASICs. Furthermore, the APEX MultiCore™ architecture, which combines LUT logic, product-term logic, and embedded memory, is ideal for system-level integration.

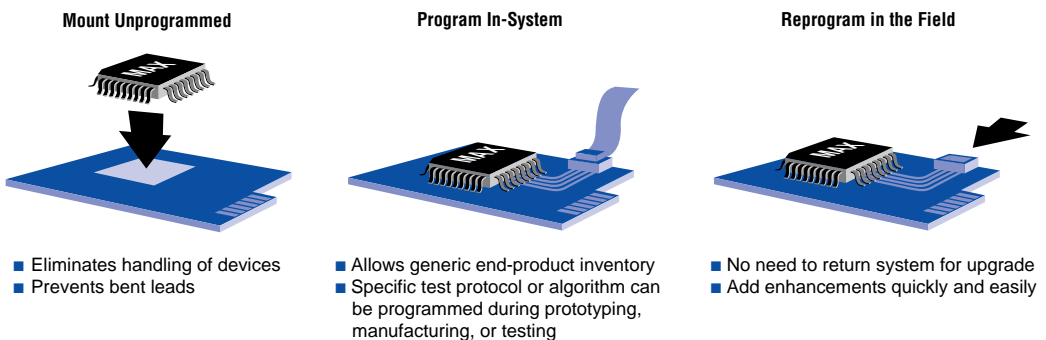
Cost-Effectiveness

Altera continually strives to refine the product development and manufacturing processes. The expertise accumulated in more than a decade of industry leadership has made both process technologies and manufacturing flow highly efficient, enabling Altera to offer the most cost-effective, highest-performance programmable logic available. Altera PLDs offer costs equivalent to gate arrays.

Shorter Development Cycles

Time is the most precious resource for many design engineers. Large sums of money are lost on projects that are not completed on schedule, thereby missing a window of opportunity in the market. Consequently, designers seek to achieve the shortest development cycle possible. Altera's fast, intuitive, and easy-to-use Quartus and MAX+PLUS II software can dramatically shorten the development cycle. With the Quartus and MAX+PLUS II software, design entry, processing, verification, and device programming together require only a few hours, potentially allowing several complete design iterations in one day. Altera also works closely with electronic design automation (EDA) manufacturers to integrate the Quartus and MAX+PLUS II software with other industry-standard design entry, synthesis, and verification tools such as those provided by Cadence, Exemplar Logic, Mentor Graphics, Synopsys, Synplicity, and Viewlogic. Figure 2 illustrates a typical PLD development cycle in the MAX+PLUS II environment.

Figure 2. ISP Increases Manufacturing Efficiency



Benefits of In-System Programmability (ISP)

In-system programmability, available in MAX[®] 9000, MAX 7000S, MAX 7000A, and MAX 3000A devices, makes prototyping easy during design development, streamlines production, increases design flexibility, and allows quick and efficient in-field upgrades. ISP uses the IEEE Std. 1149.1 Joint Action Test Group (JTAG) test port, which allows devices to be programmed and the printed circuit board (PCB) to be functionally tested in a single manufacturing step (see Figure 3).

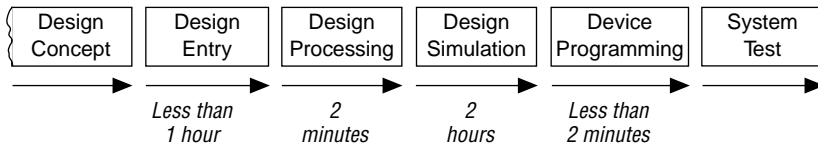
Whether a designer uses Altera's ByteBlasterMV[™] parallel port download cable during prototyping, in-circuit testers during manufacturing, or an embedded processor for field upgrades, Altera's devices and support provide an industry-standard solution through ISP for all types of applications.

Jam Programming & Test Language

The Jam[™] programming and test language addresses the issues designers face when programming PLDs in-system. These issues include proprietary file formats, vendor-specific programming algorithms, large file sizes, and long programming times. The Jam language is a major step forward in providing a software-level standard for in-system programming. For more information on the Jam language, see "Jam Programming & Test Language" on page 20.

Figure 3. Altera PLD Development Cycle Using the Quartus & MAX+PLUS II Software

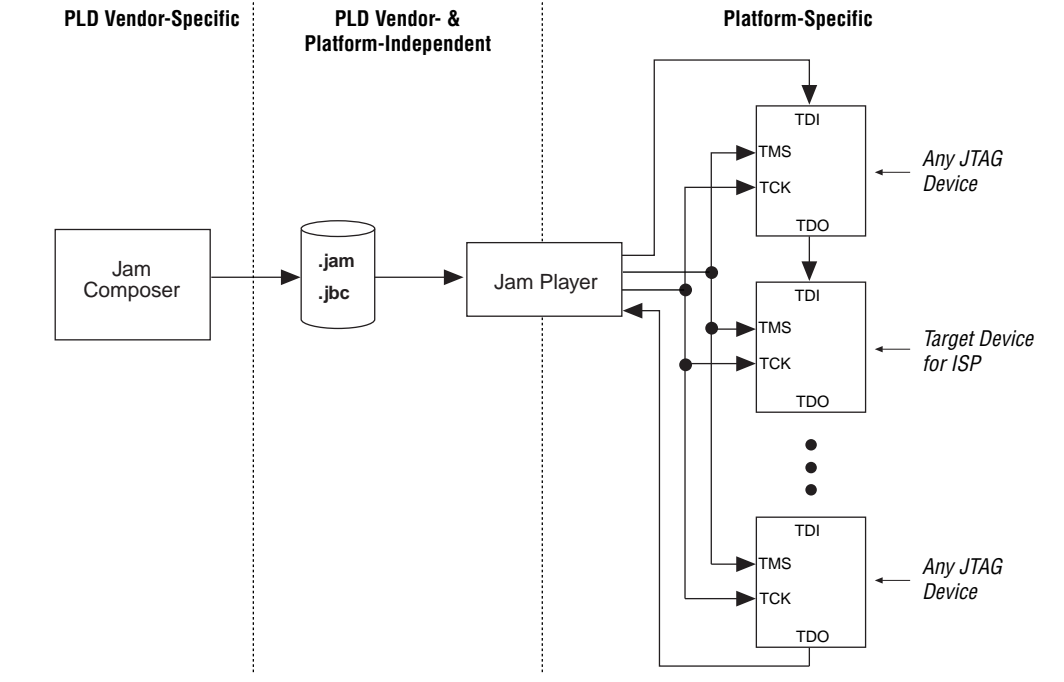
The times shown are representative of a relatively sophisticated 10,000-gate logic design.



The Jam standard is a vendor- and platform-independent interpreted language optimized for programming devices via the IEEE Std. 1149.1 (JTAG) interface. The Jam language allows a single Jam File (**.jam**) or Jam Byte-Code file (**.jbc**) to contain both the data to be programmed into a device and the algorithm required to accomplish programming.

The Jam programming solution consists of two software components: the Jam Composer and the Jam Player. The Jam Composer writes the Jam File that contains the user data and programming algorithm required to program a design into a device. The Jam Player interprets the Jam File and manages the JTAG port to program devices. The Jam instruction set includes JTAG-based and algorithmic instructions. These elements create a universal language and tool set that addresses all PLDs and programming methodologies. Figure 4 describes a basic Jam flow.

Figure 4. Basic Jam Flow



For more information on the Jam programming and test language, see the *Jam Programming & Test Language Specification* or go to the Jam web site at <http://www.jamisp.com>.

Altera Device Families

Altera offers the following families of general-purpose PLDs: APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 5000, and Classic™ devices (see Table 2). The Flexible Logic Element MatriX (FLEX) architectures use look-up tables (LUTs) to implement logic functions, whereas the Multiple Array MatriX (MAX) and Classic architectures use a programmable-AND/fixed-OR product-term architecture. The Advanced Programmable Logic MatriX (APEX) architecture combines LUTs and product terms. Each device family offers unique features as well as distinct speed and utilization advantages for implementing particular applications.

Table 2. Altera Device Architectures

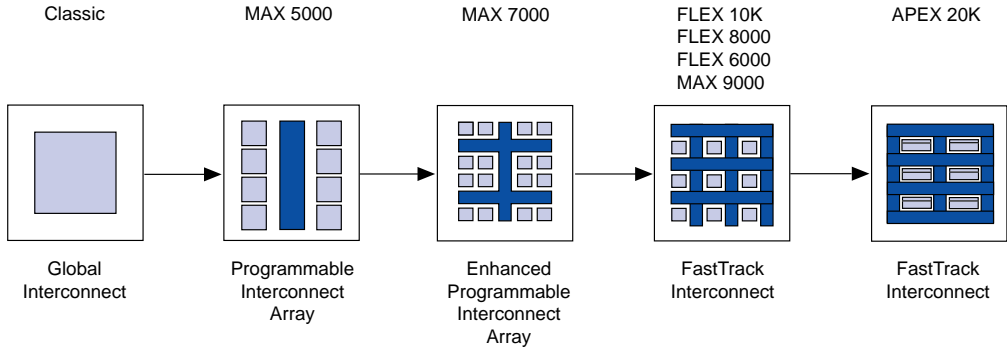
Device Family	Logic Cell Structure	Interconnect Structure	Reconfigurable Element
APEX 20K	Look-up table and product-term	Continuous	SRAM
FLEX 10K	Look-up table	Continuous	SRAM
FLEX 8000	Look-up table	Continuous	SRAM
FLEX 6000	Look-up table	Continuous	SRAM
MAX 9000	Product term	Continuous	EEPROM
MAX 7000	Product term	Continuous	EEPROM
MAX 5000	Product term	Continuous	EPROM
Classic	Product term	Continuous	EPROM

Table 3 shows the range of user I/O pins and typical gates for each device family.

Table 3. User I/O Pins & Usable Gates of Altera Device Families

Device Family	User I/O Pins	Typical Usable Gates
APEX 20K	250 to 780	263,000 to 2,670,000
FLEX 10K	59 to 470	10,000 to 250,000
FLEX 8000	68 to 208	2,500 to 16,000
FLEX 6000	71 to 218	16,000 to 24,000
MAX 9000	52 to 216	10,000 to 12,000
MAX 7000	36 to 212	600 to 10,000
MAX 5000	28 to 100	600 to 3,750
Classic	22 to 68	300 to 900

Figure 5 summarizes the Altera device architecture and illustrates how the interconnect structure has evolved to maintain high performance even at the highest densities.

Figure 5. Altera Architecture Evolution

All Altera device families are fabricated on CMOS processes. As part of Altera's commitment to continual improvement, devices are transferred to advanced process technologies as soon as they become viable and can support reliable manufacturing. This transfer generally reduces manufacturing costs and enhances performance, producing faster, more cost-effective devices. The following sections summarize the key features and benefits of Altera's general-purpose PLD families.

APEX 20K Device Family

The APEX 20K device family features the MultiCore architecture, which includes a combination of LUTs, product terms, and memory to enable effective integration of a wide variety of system sub-functions, including processing, memory, and interface functions on a single chip. The APEX 20K family will include seven devices with typical gate counts ranging from 100,000 gates to 1 million gates.

The APEX 20K device family is supported by the Quartus software, Altera's fourth-generation programmable logic design tool. The Quartus development tool is specially developed to support million-plus gate designs in work group environments including internet-based collaborative efforts and HDL-based intellectual property (IP) for faster time-to-market. The Quartus software is fully compatible with tools from Cadence, Exemplar Logic, Mentor Graphics, Synopsis, Synplicity, and other leading EDA vendors.

The APEX 20K architecture combines logic elements (LEs) and ESB into large blocks called MegaLAB™ structures, which are connected throughout the device via Altera's four-level continuous FastTrack® Interconnect routing structure. Each ESB has 2,048 programmable bits, which can be configured to support RAM, ROM, or content-addressable memory (CAM). Additionally, the ESB provides the product-term capability of the MultiCore architecture.

FLEX 10K Device Family

The FLEX 10K device family features the first PLDs to contain embedded arrays with up to 250,000 gates. The FLEX 10K family, which includes FLEX 10KA and FLEX 10KE devices, can address the increasing levels of integration needed to accommodate system-level designs with their high density and ability to implement complex megafunctions and memories in designs. Each FLEX 10K device contains an embedded array, which gives designers the efficiency of embedded gate arrays and the flexibility of programmable logic. The embedded array is composed of a series of embedded array blocks (EABs), which can be used to implement various memory and complex logic functions. In addition, FLEX 10K devices can be reconfigured in-circuit via an external configuration device or intelligent controller. The devices also offer MultiVolt™ I/O interface operation, which allows a device to bridge between systems operating at different voltages. Other architectural features— such as multiple low-skew clocks, ClockLock™ and ClockBoost™ phase-locked loop (PLL) circuitry, and internal tri-state buses—provide the performance and efficiency required for system-level integration. These features make FLEX 10K devices ideal for applications that have been traditionally reserved for gate arrays.

The 2.5-V, 0.25- μ m FLEX 10KE devices support efficient implementation of dual-port RAM and further enhance the performance of the FLEX 10K family. Designed for compliance with the 3.3-V peripheral component interconnect (PCI) specification, FLEX 10KE devices are an average of 20%-30% faster than the equivalent 3.3 V, 0.35 μ m FLEX 10KA devices. FLEX 10KE devices range in density from 30,000 to 200,000 gates.

FLEX 8000 Device Family

The FLEX 8000 device family is ideal for applications that require a large number of registers and I/O pins. Devices in this family range in density from 2,500 to 16,000 usable gates, with 282 to 1,500 registers, and 68 to 208 user I/O pins. FLEX 8000 devices can be reconfigured in-circuit via an external configuration device or intelligent controller, and offer MultiVolt I/O interface operation, which allows a device to bridge between systems operating at different voltages. These features, along with a high-performance and predictable interconnect structure, make FLEX 8000 devices as easy to use as product-term-based devices. In addition, SRAM-based FLEX 8000 devices provide low standby power and can be reconfigured in-circuit, making them ideal for such applications as PC add-on cards, battery-powered instruments, and multi-purpose telecommunication cards.

FLEX 6000 Device Family

The FLEX 6000 device family provides a low-cost programmable alternative to gate arrays for high-volume designs. FLEX 6000 devices are based on the OptiFLEX™ architecture, which is made up of LEs that each have a 4-input LUT, a register, and dedicated paths for carry and cascade chain functions. LEs are combined into groups called logic array blocks (LABs); each LAB contains 10 LEs. FLEX 6000 devices also have reconfigurable SRAM elements, which give designers the flexibility to change their designs quickly during prototyping and design testing. Devices in this family offer 10,000 to 24,000 gates, 880 to 1,960 LEs, and 71 to 218 user I/O pins. In addition, FLEX 6000 devices can be reconfigured in-circuit via an external configuration device or intelligent controller, and offer MultiVolt I/O interface operation.

MAX 9000 Device Family

The MAX 9000 device family combines the efficient macrocell architecture of MAX 7000 devices with the high-performance, predictable FastTrack Interconnect of FLEX devices, resulting in a device family that is ideal for integrating multiple system-level functions. The EEPROM-based MAX 9000 device family ranges from 6,000 to 12,000 usable gates, 320 to 560 macrocells, and 52 to 216 user I/O pins. This level of density makes the MAX 9000 device family an ideal choice for gate array designs that need the benefits of PLDs and the flexibility of ISP. MAX 9000 devices are in-system programmable via an industry-standard 4-pin JTAG interface.

MAX 7000 Device Family

The MAX 7000 device family is the fastest high-density programmable logic family in the industry. The MAX 7000 device family—which includes MAX 7000, MAX 7000S, and MAX 7000A devices—ranges in density from 600 to 10,000 usable gates, 32 to 512 macrocells, and 36 to 212 user I/O pins. These EEPROM-based devices offer combinatorial propagation delays as fast as 4.5 ns and 16-bit counter frequencies as fast as 192.3 MHz. Moreover, they provide very fast input register setup times, multiple system clocks, and a programmable speed/power control. MAX 7000E devices are the higher-density, feature-enhanced members of the MAX 7000 family. MAX 7000S devices provide the enhanced features of MAX 7000E devices, as well as support for JTAG boundary-scan test (BST) circuitry and ISP. MAX 7000S devices are in-system programmable via an industry-standard 4-pin JTAG interface.

MAX 7000A devices support 3.3-V ISP through the built-in IEEE Std. 1149.1 (JTAG) interface with advanced pin-locking capability. The devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency. Other architectural features include a programmable slew rate control, six pin-or logic-driven output enable signals, very fast input register setup times, MultiVolt I/O interface capability, and configurable expander product-term distribution, allowing up to 32 product terms in each macrocell.

MAX 5000 Device Family

The MAX 5000 device family provides a comprehensive, cost-effective solution for designs that require a high level of combinatorial logic. MAX 5000 devices provide logic densities ranging from 600 to 3,750 usable gates, and I/O counts ranging from 28 to 100 pins. The EPROM-based MAX 5000 devices are nonvolatile and erasable. Altera's continuing commitment to migrating existing families to newer, more aggressive technologies has yielded MAX 5000 devices that offer excellent cost-per-macrocell values.

MAX 3000A Device Family

The MAX 3000A device family is Altera's low cost, high-density programmable logic family and ranges in density from 600 to 5,000 usable gates, 32 to 256 macrocells, and 34 to 158 user I/O pins. These EEPROM-based devices offer combinatorial propagation delays as fast as 4.5 ns and 16-bit counter frequencies as fast as 192.3 MHz. Moreover, they provide multiple system clocks, and a programmable speed/power control. MAX 3000A devices provide support for JTAG BST circuitry and ISP. MAX 3000A devices are in-system programmable via an industry-standard 4-pin JTAG interface. These devices also support hot-socketing and the MultiVolt interface, enabling the device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels.

Classic Device Family

The Classic device family is Altera's first family of devices. The EPROM-based Classic devices feature densities of up to 900 usable gates and pin counts of up to 68 pins. Composed of single arrays of globally interconnected logic, the industry-standard Classic device family offers a low-cost solution for low-density applications. Classic devices offer a unique "zero-power" mode, allowing the devices to draw only microamps of current at standby, which makes them ideal for low-power applications.

Development Tools

Altera offers the fastest, most powerful, and most flexible programmable logic development software in the industry. The Altera Quartus and MAX+PLUS II development tools provide a broad range of features with an easy-to-use graphical user interface. Both offer interfaces to industry-standard EDA tools that allow easy integration with your chosen design environment.

Design Flow

The Quartus and MAX+PLUS II software offer a full spectrum of logic design capabilities. Designers are free to combine text, graphic, and waveform design entry methods while creating hierarchical single- or multi-device designs. The Compiler performs minimization and logic synthesis, fits the design into one or more devices, and generates programming or configuration data. Design verification with functional and timing simulation and delay prediction for speed-critical paths are available, as well as multi-device simulation across multiple device families. Altera and a number of programming hardware manufacturers offer hardware for programming the devices (see Figure 6).

Quartus Development Tool

Altera's powerful fourth-generation software meets the challenges of designing for million-plus gate devices such as the new Altera APEX 20K device family. To cope with shrinking design cycles and increasing design complexity, the Quartus software includes the following state-of-the-art features: work group computing, integrated logic analysis functionality, EDA tool integration, multi-processor support, incremental recompilation, and IP integration.

The Quartus software is also "web-aware", with the latest internet technology built in. From within the software, designers have direct access over the internet to the Altera Technical Support (AtlasSM) Solutions data base to find immediate solutions for common design problems. For more specific issues, designers can submit service requests on-line directly to Altera Applications, attaching their design files to the request so that the Altera engineer assigned to the issue can accurately duplicate the design environment and find a solution.

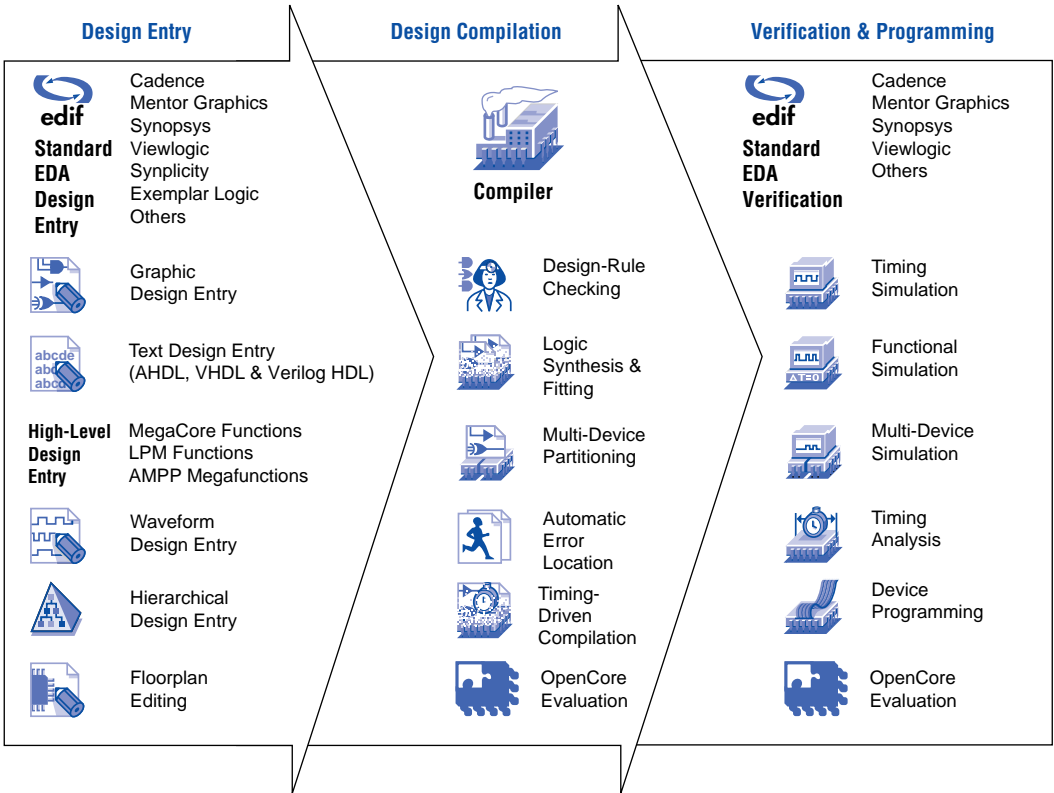
MAX+PLUS II Development Tool

Altera achieves maximum device performance and density with advanced process technologies, innovative logic architectures, and state-of-the-art design tools. The MAX+PLUS II programmable logic development system provide an architecture-independent design environment and ensures easy design entry, fast compilation, and uncomplicated device programming. The MAX+PLUS II software supports design implementation for the FLEX, MAX, and Classic device families.

With the MAX+PLUS II software, designers no longer need to master the complexities of device architectures. The MAX+PLUS II software translates designs—created with familiar design entry tools such as high-level behavioral languages schematic capture tools or—into the format required by the target architecture.

The extensive architectural knowledge built into Altera development tools minimizes the need for designers to manually optimize their designs, which allows designers to complete designs quickly. With the MAX+PLUS II software, users can take a logic circuit from design entry to device programming in a matter of hours. Design compilation is typically completed in minutes, allowing several complete design iterations to be performed in a single day.

Figure 6. Altera Design Environment



Multi-Platforms & EDA Tool Support

Altera is committed to supporting the logic development environments that are most familiar to circuit designers. The Quartus and MAX+PLUS II software provides interfaces to a wide variety of EDA tools from companies such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Viewlogic. The MAX+PLUS II software shares info with these EDA tools via EDIF Netlist Files, SRAM Object Files (.sof), the library of parameterized modules (LPM), Verilog HDL, VHDL, and DesignWare components. The MAX+PLUS II Compiler runs on PCs and UNIX workstations, making the MAX+PLUS II software the industry's only platform-independent, architecture-independent programmable logic design environment. The Altera Commitment to Cooperative Engineering Solutions (ACCESSSM) alliance, which Altera has formed with industry-leading EDA tool vendors, ensures smooth interfaces between Altera EDA tools and timely support of Altera devices with these tools.

The NativeLink feature of the Quartus software gives tight integration between the Quartus software and other design tools. Other tools can directly call the Quartus tool for design compilation, or the Quartus tool can call other tools for synthesis simulation.

Megafunctions Optimized for Altera Devices

With PLD densities reaching as high as 250,000 gates, it is now possible to implement entire digital sub-systems within a single programmable device. To facilitate this high level of integration and to further reduce design cycles, Altera provides MegaCoreTM functions and supports Altera Megafunction Partners Program (AMPSM) megafunctions. Megafunctions are off-the-shelf building blocks that implement useful functions such as processors, digital signal processing (DSP) functions, bus controllers, and interfaces. Megafunctions provide a higher degree of flexibility and performance not attainable in fixed-function devices, e.g., high-speed finite impulse response (FIR) filters, and are targeted to a variety of applications, including:

- Bus protocols, including 64-bit, 66-MHz peripheral component interconnect (PCI) buses
- DSP
- Image processing
- High-speed networking, including asynchronous transfer mode (ATM) functions
- Microprocessors and microperipherals

Altera MegaCore functions are pre-verified hardware description language (HDL) design files for complex system-level functions. MegaCore functions range from standard building blocks, such as universal asynchronous receivers/transmitters (UARTs) and controllers, to innovative design examples that exploit the features of PLDs. Altera devices and development tools support both Altera-supplied MegaCore functions and functions created by AMPP partners.

MegaCore and AMPP megafunctions can be previewed before licensing via the MAX+PLUS II OpenCore™ feature. This pre-licensing evaluation system allows designers to instantiate and simulate megafunctions. However, programming files as well as output files for third-party EDA tool simulation can only be generated with an authorization code provided upon licensing.

Altera also offers the Altera Consultants Alliance Program (ACAPSM) which provides expert design assistance to designers of Altera PLD's. ACAP consultants should be used in situations where the project is not completely defined, is in transition, or cannot be successfully solved by using megafunctions alone. In these situations, an ACAP consultant with a specific specialization can respond to changes and modification requests in real-time.



For more ACAP information, go to the Altera world-wide web site at <http://www.altera.com>.

Conclusion

With the increasing trend toward System-on-a-Programmable-Chip integration, designers are challenged with producing high quality products faster and at lower costs. The advanced architectures and process technologies used in Altera devices provide the greatest performance, highest density, and greatest flexibility available in the programmable logic market. Regardless of an application's requirements, Altera devices provide an efficient solution with high levels of integration, high I/O capabilities, and the fastest speeds available.

The Quartus and MAX+PLUS II development tools give designers the ability to take full advantage of all the features offered in Altera's APEX, FLEX, MAX, and Classic devices. The advanced Quartus development software works with the APEX 20K device family and offers advanced features essential for programming million-plus gate designs including multi-processor support, incremental compilation, block-level editing, and work-group computing. The MAX+PLUS II software can target a project to the FLEX, MAX, and Classic device families, offering designers architecture-independent design capabilities, regardless of their preferred design flow.

Altera offers MegaCore functions, AMPP megafunctions, and EDA tool support, all of which contribute to Altera's total design solution. MegaCore functions and AMPP megafunctions help facilitate a higher-level of integration by reducing design cycles. Through the Quartus and MAX+PLUS II software, designers can interface with a wide variety of EDA tools that are most familiar to them.

The Jam programming and test language, compatible with all current PLDs that offer ISP, provides a software-level standard for in-system programming by remaining vendor-independent, which results in small file sizes and reduces programming times. Designers, using the Jam language to implement ISP, can lengthen the life and enhance the quality and flexibility of the end product, as well as reduce device inventories by eliminating the need to stock and track programmed devices.



Notes: